

United States Patent and Trademark Office



APPLICATION NO.		FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/065,296		10/01/2002	Liang-Hua Lin	NAUP0477USA	5720
27765	7590	10/31/2003		EXAMINER	
•		MERICA INTER	HUYNH, YENNHU B		
	P.O. BOX 506 MERRIFIELD, VA 22116				PAPER NUMBER
	,			2813	
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DATE MAILED: 10/31/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

		(K)						
	Application No.	Applicant(s)						
Office Anti-u Common to	10/065,296	LIN ET AL.						
Office Action Summary	Examiner	Art Unit						
The MAN INC DATE - 64big	Yennhu B Huynh	2813						
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply								
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). - Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b). Status								
1) Responsive to communication(s) filed on 14 A	<u> Nugust 2003</u> .							
2a)☐ This action is FINAL . 2b)⊠ Thi	is action is non-final.							
3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is								
closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213. Disposition of Claims								
4)⊠ Claim(s) <u>1-10</u> is/are pending in the application.								
4a) Of the above claim(s) is/are withdrawn from consideration.								
5) Claim(s) is/are allowed.								
6)⊠ Claim(s) <u>1-10</u> is/are rejected.								
	7) Claim(s) is/are objected to.							
8) Claim(s) are subject to restriction and/or election requirement.								
Application Papers								
9)☐ The specification is objected to by the Examiner. 10)☐ The drawing(s) filed on is/are: a)☐ accepted or b)☐ objected to by the Examiner.								
	'							
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a). 11) The proposed drawing correction filed on is: a) approved b) disapproved by the Examiner.								
If approved, corrected drawings are required in reply to this Office action.								
12) The oath or declaration is objected to by the Examiner.								
Priority under 35 U.S.C. §§ 119 and 120								
13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).								
a) ☐ All b) ☐ Some * c) ☐ None of:								
1. Certified copies of the priority documents have been received.								
2. Certified copies of the priority documents have been received in Application No								
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. 								
14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).								
a) ☐ The translation of the foreign language provisional application has been received. 15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.								
Attachment(s)								
1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO-1449) Paper No(s)	5) Notice of Informal	y (PTO-413) Paper No(s) Patent Application (PTO-152)						

U.S. Patent and Trademark Office PTOL-326 (Rev. 04-01)

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DETAILED ACTION

The Office Action is in response to the Amendment A filed on 8/14/03.

Election/Restrictions

Applicant's election without traverse of claims 1-10 in Paper No. 3 is acknowledged.

Claims 11-19 are cancelled by the Amendment A filed on 8/14/03.

Specification

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Method Of Forming A Photo Sensor On Semiconductor Wafer With Overlapped Region.

Claim Objections

Claim 1 is objected to because of the following informalities:

In claim 1, lines 5 & 9, the recited limitation --a surface of the substrate-- should be changed to --the surface of the substrate--.

Appropriate correction is required.

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Claim Rejections - 35 USC § 112

Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, the recited limitation: "a first ion implantation process utilizing second type dopants to form a plurality of first doped regions on a surface of the photo sensor". It is un clear. Without a predetermined pattern or a photo resist etching step performance to define the plurality regions of the photo sensor area, how a **plurality** of first doped regions is formed on the surface of the photo sensor.

Appropriated correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1,2,4, 7 & 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuo et al. (U.S. 6,448,101B1) in view of Rhodes (U.S. 6,611,037B1).

Kuo et al. at figs 1-10 in related text col. 1-6 disclose a method of integrating a photodiode, which include:

-Re. claims 1 & 2: a photo sensor area 12 in a photo diode 35 formed on a semiconductor wafer 10 with first P type dopants semiconductor substrate surface;

insulating/STI 26 surrounding the photo sensor; performing a first ion implantation process with the second N type dopants to form a first doped region 18 on the surface of the photo sensor; and a second ion implantation with second N type dopants to form a second doped region 30 being overlapped portion of the first doped region 18 (col.2 & 3, lines 53-), wherein the dopants in the first and second doped region interact with neighboring substrate to form depleted region (col.3, lines 17-22).

However, Kuo et al. do not disclose wherein the first ion implantation forming a plurality of the first doped region on the surface of the photo sensor.

Rhodes at figs. 1-15 in related text col. 1-14 disclose the first ion implantation forming a plurality of the first doped regions on the surface of the photo sensor (col.4, lines 41-46 and col. 8, lines 18-37).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Kuo et al. invention by incorporation a plurality of the first doped regions forming, to increase the contacting area between the doped regions and substrate, so that the sensing area of the photo diode is effectively increased.

Kuo et al. also disclose:

-Re. claim 4: wherein the first type dopants are P type and the second type dopant is N type (col. 2 & 3, lines 50-21).

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-Re. claim 7: wherein the surface of the semiconductor wafer comprises a logic circuit region 14, and the second ion implantation process forms at least a lightly doped drain and source area 40 & 42 within the logic circuit (col.4, lines 7-19).

-Re. claim 10: wherein the second N doped region 31 is utilized to be a conducting wire /bit line of the photo sensor (col.3, lines 20,21).

Claims 3,5 & 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuo et al. (U.S. 6,448,101B1) in view of Rhodes (U.S. 6,611,037B1) and Rhode et al. (U.S. 6,534,335B1).

Kuo et al. and Rhodes ('037B1) disclose substantially all of the claimed invention, but do not disclose wherein the first type dopants are N type and the second type dopant is P type (cl. 3).

Re. claim 3: Rhodes et al. ('335B1) in related text disclose optimized low leakage photodiodes, which include a first type dopants are N/P type and the second type dopant are P/N type which related to N or P type semiconductor substrate conductive respectively (col.7, lines 26-43).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Kuo et al. and Rhodes ('037B1) invention by incorporation the first N type dopants and the second P type dopants that are related to P or N semiconductor substrate conductive type respectively or the like, which can be utilized in forming the regions or junctions in the base semiconductor, and prevent cross talk affect.

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Kuo et al. and Rhodes ('037B1) also do not disclose also do not disclose wherein the substrate comprises an epitaxial silicon layer and each of the first and second doped region are formed inside the epitaxial silicon layer (cl.5).

-Re. claim 5: Rhodes et al. ('335B1) also disclose wherein the substrate 112 of a photo sensor comprises an epitaxial silicon layer on the semiconductor substrate and each of the first N type doped region 130 and second N type doped region 110 are formed inside the epitaxial silicon layer (fig. 3, col.3 lines 15-26).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Kuo et al. and Rhodes ('037B1) invention by incorporation epitaxial silicon layer on the semiconductor substrate, to obtain a supported layer in forming regions or junctions, in the base semiconductor structure or foundation.

Kuo et al. and Rhodes ('037B1) also do not disclose wherein the dopant density of the first ion implantation is less than the second ion implantation in process (cl.6).

Re. claim 6: Rhodes et al. ('335B1) also disclose the dopant density/dopant concentration of the first ion implantation region 130 is less than the second ion implantation region 110 in process (fig.3, col.4, lines 15-44).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Kuo et al. and Rhodes ('037B1) invention by incorporation the dopant concentration/density of the first ion implantation is less than

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the second ion implantation, to obtain a width of depletion region/junction depth/or a shallow penetration depth which can be expended and sensitivity of the photo diode for detecting blue light can be enhanced.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kuo et al. (U.S. 6,448,101B1) in view of Rhodes (U.S. 6,611,037B1) and Chen et al. (U.S. 2003/0085415 A1).

Kuo et al. and Rhodes et al. disclose substantially all of the claimed invention, but do not disclose a capacitance of depletion region is approximately equal to zero for increasing sensing area, decreasing dark current and further increasing photo current and photon conversion gain.

-Re. claim 9: Chen et al. in related text disclose CMOS image sensor device.

Chan et al. do not state that a capacitance of depletion region is approximately equal to zero for increasing sensing area, but indicate that wherein the depletion region receives photons and produce junction current by transforming photons into electrons, and receives a quantity of photons which is photon conversion gain to increasing the sensing area (p.1 [0018] and p.2, cl.10).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Kuo et al. and Rhodes invention by incorporation the depletion region receives a quantity photons and produces junction current by

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transforming photons into electrons, such that the dark current is decreased and the sensor device is enhanced.

Allowable Subject Matter

Claim 8 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for allowance: prior art does not disclose a method of forming photo sensor, which includes an annealing process for driving-in the dopants in the second doped region.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue-fee. Such-submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yennhu B Huynh whose telephone number is 703-308-6110. The examiner can normally be reached on 8.30AM-7.00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached on 703-308-4940. The fax phone numbers for the organization where this application or proceeding is assigned are 703-

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308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-7724.

Yennhu Huynh Examiner 10/26/03 y